

**What is claimed is:**

1        1. A method of forming a CMOS thin film transistor device  
2        on a substrate having an NMOS area, a PMOS area and a circuit  
3        area, the NMOS area having a first doped area, a lightly doped  
4        area and a first gate area, and the PMOS area having a second  
5        doped area and a second gate area, the method comprising the  
6        steps of:

- 7              (a) forming a semiconductor layer on the substrate;  
8              (b) performing a first patterning process using a first  
9                photomask on the semiconductor layer to form a first  
10          semiconductor island and a second semiconductor  
11          island on part of the substrate, wherein the first  
12          semiconductor island is located in the NMOS area and  
13          the second semiconductor island is located in the  
14          PMOS area;  
15          (c) forming a dielectric layer on the first semiconductor  
16          island, the second semiconductor island and the  
17          substrate;  
18          (d) forming a metal layer on the dielectric layer;  
19          (e) performing a second patterning process using a second  
20          photomask to form a first photoresist layer on the  
21          metal layer located in the lightly doped area, the  
22          first gate area, the PMOS area and the circuit area;  
23          (f) using the first photoresist layer as a mask, removing  
24          part of the metal layer to form a first metal layer  
25          in the lightly doped area and the first gate area,  
26          a second metal layer in the PMOS area and a third  
27          metal layer in the circuit area, wherein the third

28               metal layer electrically connects the first metal  
29               layer and the second metal layer;

30               (g) using the first and the second metal layers as masks,  
31               performing an n<sup>+</sup>-ion implantation to form a first  
32               source/drain region in the first semiconductor island  
33               in the first doped area;

34               (h) performing a dry etching procedure to remove part of  
35               the first photoresist layer, part of the first metal  
36               layer and part of the second metal layer, thus forming  
37               a first gate with a symmetrical cone shape, a remaining  
38               second metal layer and a remaining first photoresist  
39               layer, and exposing the dielectric layer in the  
40               lightly doped area, wherein a bottom width of the  
41               first gate is narrower than that of the first metal  
42               layer, and the symmetrically coned shape is gradually  
43               thinner from bottom to top;

44               (i) using the first gate and the remaining second metal layer  
45               as masks, performing an n<sup>-</sup>-ion implantation to form  
46               an LDD (lightly doped drain) region in the first  
47               semiconductor layer in the lightly doped area;

48               (j) removing the remaining first photoresist layer and thus  
49               forming an NMOS element in the NMOS area;

50               (k) performing a third patterning process using a third  
51               photomask to remove the remaining second metal layer  
52               in the second doped area, thus forming a second gate  
53               on the dielectric layer in the second gate area; and

54               (l) performing a p<sup>+</sup>-ion implantation to form a second  
55               source/drain region in the second semiconductor  
56               island in the second doped area, thus forming a PMOS  
57               element in the PMOS area.

1       2. The method according to claim 1, wherein step (k)  
2 further comprises the steps of:

3           (k1) performing the third patterning process using the third  
4           photomask to form a second photoresist layer cover  
5           the NMOS area, the circuit area and the second gate  
6           area; and

7           (k2) using the second photoresist layer as a mask, removing  
8           the remaining second metal layer in the second doped  
9           area to form the second gate on the dielectric layer  
10          in the second gate area.

1       3. The method according to claim 2, wherein step (l)  
2 further comprises the step of:

3           (l1) using the second photoresist layer and the second gate  
4           as masks, performing the p<sup>+</sup>-ion implantation to form  
5           the second source/drain region in the second  
6           semiconductor island in the second doped area and  
7           thus forming the PMOS element in the PMOS area.

1       4. The method according to claim 1, wherein the substrate  
2 is a glass substrate.

1       5. The method according to claim 1, wherein the first  
2 and the second semiconductor islands comprise silicon.

1       6. The method according to claim 1, wherein the dielectric  
2 layer is a SiO<sub>x</sub> layer.

1       7. The method according to claim 1, wherein the metal  
2 layer comprises Mo.

1        8. The method according to claim 1, wherein part of the  
2 metal layer is removed by dry or wet etching.

1        9. The method according to claim 1, wherein an included  
2 angle at the bottom of the symmetrically coned shape is less  
3 than 45°.

1        10. The method according to claim 1, wherein an etching  
2 selectivity of the first photoresist layer to the metal layer  
3 ranges from 1 to 1/4.

1        11. A method of forming a CMOS thin film transistor device  
2 on a glass substrate having an NMOS area, a PMOS area and a circuit  
3 area, the NMOS area having a first doped area, a lightly doped  
4 area and a first gate area, and the PMOS area having a second  
5 doped area and a second gate area, the method comprising the  
6 steps of:

- 7        (a) forming a semiconductor layer on the substrate;
- 8        (b) performing a first patterning process using a first  
9              photomask on the semiconductor layer to form a first  
10          semiconductor island and a second semiconductor  
11          island on part of the glass substrate, wherein the  
12          first semiconductor island is located in the NMOS  
13          area and the second semiconductor island is located  
14          in the PMOS area;
- 15        (c) forming a silicon oxide ( $\text{SiO}_x$ ) layer on the first  
16          semiconductor island, the second semiconductor  
17          island and the glass substrate;
- 18        (d) forming a molybdenum (Mo) layer on the silicon oxide  
19          layer;

20                         (e) performing a second patterning process using a second  
21                         photomask to form a first photoresist layer on the  
22                         Mo layer located in the lightly doped area, the first  
23                         gate area, the PMOS area and the circuit area;  
24                         (f) using the first photoresist layer as a mask, removing  
25                         part of the Mo layer to form a first Mo layer in the  
26                         lightly doped area and the first gate area, a second  
27                         Mo layer in the PMOS area and a third Mo layer in  
28                         the circuit area, wherein the third Mo layer  
29                         electrically connects the first Mo layer and the  
30                         second Mo layer;  
31                         (g) using the first and the second Mo layers as masks,  
32                         performing an n<sup>+</sup>-ion implantation to form a first  
33                         source/drain region in the first semiconductor island  
34                         in the first doped area;  
35                         (h) performing a dry etching procedure to remove part of  
36                         the first photoresist layer, part of the first Mo  
37                         layer and part of the second Mo layer, thus forming  
38                         a first gate with a symmetrical cone shape, a remaining  
39                         second Mo layer and a remaining first photoresist  
40                         layer, and exposing the silicon oxide layer in the  
41                         lightly doped area, wherein a bottom width of the  
42                         first gate is narrower than that of the first metal  
43                         layer, and the symmetrically coned shape is gradually  
44                         thinner from bottom to top;  
45                         (i) using the first gate and the remaining second Mo layer  
46                         as masks, performing an n<sup>-</sup>-ions implantation to form  
47                         an LDD (lightly doped drain) region in the first  
48                         semiconductor layer in the lightly doped area;

49                 (j) removing the remaining first photoresist layer and thus  
50                         forming an NMOS element in the NMOS area;  
51                 (k) performing a third patterning process using a third  
52                         photomask to remove the remaining second Mo layer  
53                         in the second doped area to form a second gate on  
54                         the silicon oxide layer in the second gate area; and  
55                 (l) performing a p<sup>+</sup>-ion implantation to form a second  
56                         source/drain region in the second semiconductor  
57                         island in the second doped area, thus forming a PMOS  
58                         element in the PMOS area.

1                 12. The method according to claim 11, wherein step (k)  
2 further comprises the steps of:

3                 (k1) performing the third patterning process using the third  
4                         photomask to form a second photoresist layer cover  
5                         the NMOS area, the circuit area and the second gate  
6                         area; and  
7                 (k2) using the second photoresist layer as a mask, removing  
8                         the remaining second Mo layer in the second doped  
9                         area to form the second gate on the silicon oxide  
10                         layer in the second gate area.

1                 13. The method according to claim 12, wherein step (l)  
2 further comprises the step of:

3                 (l1) using the second photoresist layer and the second gate  
4                         as masks, performing the p<sup>+</sup>-ion implantation to form  
5                         the second source/drain region in the second  
6                         semiconductor island in the second doped area and  
7                         thus forming the PMOS element in the PMOS area.

1        14. The method according to claim 11, wherein the first  
2 and the second semiconductor islands are polysilicon layers.

1        15. The method according to claim 11, wherein part of the  
2 metal layer is removed by dry or wet etching.

1        16. The method according to claim 11, wherein an included  
2 angle at the bottom of the symmetrical cone shape is less than  
3 45°.

1        17. The method according to claim 11, wherein an etching  
2 selectivity of the first photoresist layer to the metal layer  
3 ranges from 1 to 1/4.

1        18. A method of forming a CMOS thin film transistor device  
2 on a substrate having at least one NMOS area, the NMOS area having  
3 a doped area, a lightly doped area and a gate area, the method  
4 comprising the steps of:

- 5            (a) forming a semiconductor layer on the substrate;
- 6            (b) patterning the semiconductor layer to form a  
7                semiconductor island in the NMOS area;
- 8            (c) forming a dielectric layer on the semiconductor island  
9                and the substrate;
- 10          (d) forming a metal layer on the dielectric layer;
- 11          (e) removing part of the metal layer to form a first metal  
12                layer in the lightly doped area and the gate area;
- 13          (f) using the first metal layer as a mask, performing an  
14                 $n^+$ -ion implantation to form a source/drain region  
15                in the semiconductor island in the doped area;
- 16          (g) performing a dry etching procedure to remove part of  
17                the first metal layer, thus forming a gate with a

18               symmetrical cone shape and exposing the dielectric  
19               layer in the lightly doped area, wherein a bottom  
20               width of the gate is narrower than that of the metal  
21               layer, and the symmetrical cone shape is gradually  
22               thinner from bottom to top; and

23               (h) using the gate as a mask, performing an n<sup>-</sup>-ion  
24               implantation to form an LDD (lightly doped drain)  
25               region in the semiconductor layer in the lightly doped  
26               area, and thus forming an NMOS element in the NMOS  
27               area.

1               19. The method according to claim 18, wherein an included  
2               angle at the bottom of the symmetrically coned shape is less  
3               than 45°.

1               20. The method according to claim 19, wherein an etching  
2               selectivity of the first photoresist layer to the metal layer  
3               ranges from 1 to 1/4.